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Claims 1-16 are presented below for examination. Claims 1, 9 and 14 are amended in this response.

1. (Currently Amended) A pipelined multistreaming processor, comprising: an instruction source;

a first cluster of a plurality of streams fetching instructions from the instruction source;

a second cluster of a plurality of streams fetching instructions from the instruction source;

dedicated instruction queues for individual streams in each cluster;

a first dedicated single dispatch stage in dedicated to the first cluster of streams for dispatching instructions from all of the streams in the first cluster of streams to execution units; and

a second dedicated single dispatch stage in dedicated to the second cluster of streams for dispatching instructions from all of the streams in the second cluster of streams to execution units;

characterized in that the clusters operate independently, with the dedicated dispatch stage taking instructions only from the instruction queues in the individual clusters to which the dispatch stages are dedicated.

- 2. (Original) The processor of claim 1 wherein individual ones or groups of execution units are associated with and dedicated for use by individual clusters.
- 3. (Original) The processor of claim 1 wherein individual streams in a cluster have dedicated fetch stages.





- 4. (Original) The processor of claim 1 wherein the total number of streams in the processor is eight, with four streams in each cluster.
- 5. (Original) The processor of claim 1 wherein instructions are fetched in each cycle for one stream in each cluster.
- 6. (Original) The processor of claim 1 wherein the a set of fetch program counters (FPC) are monitored with one FPC dedicated to each stream, and fetching of instructions is directed beginning at addresses according to the program counters.
- 7. (Original) The processor of claim 4 wherein eight instructions are fetched for a stream each time instructions are fetched for that stream.
- 8. (Original) The processor of claim 2 further comprising one or more execution units to which either or both dispatch stages may dispatch instructions.
- 9. (Currently Amended) In a pipelined multistreaming processor having an instruction source and a plurality of streams, a method for simplifying implementation and operation of the streams, comprising the steps of:
 - (a) clustering the streams into two or more clusters;
- (b) dedicating a single dispatch stage to all of the streams of each cluster, for dispatching instructions to execution units; and
- (c) fetching, in each cycle, a series of instructions from the instruction source by a single cluster.

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- 10. (Original) The method of claim 9 further comprising groups of execution units dedicated to each cluster, to which the dispatch stages in that cluster may dispatch instructions.
- 11. (Original) The method of claim 9 further comprising fetch stages dedicated to individual streams in a cluster.
- 12. (Original) The method of claim 9 wherein the total number of streams in the processor is eight, and the number of streams in each cluster is four.
- 13. (Original) The method of claim 9 having a fetch program counter (FPC) associated with each stream, wherein fetching is directed beginning at addresses according to the program counters.
- 14. (Currently Amended) The method of claim 9 wherein eight instructions are fetched each time instructions are fetched for a stream.
- 15. (Original) The method of claim 9 wherein the processor further comprises one or more general execution units, and each dispatch stage is enabled to dispatch instructions to the general execution units.
- 16. (Original) The method of claim 9 wherein each stream in each cluster has an instruction queue associated with that stream, and further comprising a step for dispatching instructions to execution units dedicated to each cluster from the instruction queues associated with the streams in each cluster.